

Title: Physical Design Engineer

Duties

- Perform RTL to GDSII design flow, including floor planning, power grid design, place and route, clock tree synthesis, timing closure, power/signal integrity signoff, EM/IR.
- Perform Full chip DRC/LVS
- Automate the design flow to promote efficiency, improve RTL to GDS design flow;
- Participate in next generation physical design, methodology and flow development.

Requirements

- BSEE/MSEE with minimum 1-year of P&R experience by using SoC Encounter.
- Successful track records of taping out 40/28/16 nm chips
- Familiar with DC,PT,DFT is prefer;.
- Be familiar with RTL to GDSII design flow;.
- Be familiar with EDA tool, such as ICC or Soc encounter;
- Be familiar with computer languages such as Perl/TCL/C-shell;
- Self-motivated with good communication skills and team spirit.