



About Credo

Credo was privately-funded until 2015 when it received its first round of Series A funding which was lead by Walden International. In 2019, Credo has four R&D centers in US Silicon Valley, Shanghai Zhangjiang High-Tech Park, Hong Kong Science & Technology Park and Taiwan Hsinchu. Credo has over 200 staff members until Mar 2019, among which 90% is R&D. Credo plans to add more members in 2019

Credo provides SerDes IP and high-speed end-to-end interconnect solutions for a wide range of applications including Data Center, Artificial Intelligent (AI), Super Computer. Since its inception, Credo has consistently delivered breakthroughs in SerDes technology including the delivery of the industry's first CMOS 50G SerDes IP based on NRZ modulation, as well as the delivery of the industry's first CMOS 100G PAM4. Credo's unique, patented mixed signal architecture is the foundation for its high performance and low power at these accelerated bandwidth rates.

Recent news to the company

Credo announced the successful interoperability of Credo's Active Ethernet Cable (AEC) connectivity solutions with Innovium's industry-leading 12.8Tbps TERALYNX™ switch silicon. The companies will demonstrate their products live at Optical Fiber Communications (OFC) Conference and Exhibition, to be held March 5-7, 2019 at the San Diego, CA Convention Center.

Credo announced it will conduct multiple product demonstrations at the 2018 China International Opto-electronic Exposition (CIOE) showcasing its new product family of Active Ethernet Cables Sep 4 2018

Credo announced it will demonstrate its advanced high performance, low power SerDes IP offerings at next week's TSMC 2018 OIP Forum and Technology Symposium in Amsterdam. Credo will be featuring single-lane rate 56G PAM4 SerDes operating in both TSMC 12nm and 7nm process technology nodes July 20 2018

Credo announced it will conduct multiple product demonstrations at Taiwan Computex showcasing its core low power, high performance 56G SerDes technology as the enabler for 200G and 400G network connectivity with exhibits taking place June 5 through June 9 2018

You can also learn more about us at www.credosemi.com.



Job Title: Physical Design Engineer

Duties

- Perform RTL to GDSII design flow, including floor planning, power grid design, place and route, clock tree synthesis, timing closure, power/signal integrity signoff, EM/IR.
- Perform Full chip DRC/LVS
- Automate the design flow to promote efficiency, improve RTL to GDS design flow;
- Participate in next generation physical design, methodology and flow development.

Requirements

- BSEE/MSEE with minimum 1-year of P&R experience by using SoC Encounter.
- Successful track records of taping out 40/28/16 nm chips
- Familiar with DC,PT,DFT is prefer;.
- Be familiar with RTL to GDSII design flow;
- Be familiar with EDA tool, such as ICC or Soc encounter;
- Be familiar with computer languages such as Perl/TCL/C-shell;
- Self-motivated with good communication skills and team spirit.

Application Method

We are looking for people with good working attitude, team spirit and strong communication skills. If you are interested in Credo and meet any requirements above, it's our pleasure to have you join our work.

Email	jobs@credosemi.com
Post	Unit 221, 2/F , Core Building 2, Phase one, Hong Kong Science Park

Only short-listed candidates will be notified.

Personal data provided by applicants will be used for recruitment purposes only.