ViXS Systems HK Ltd.
Job position: ASIC Design Engineer - Internship

Requirements:

- Verilog/VHDL coding experience is a plus
- Hands on experience with ASIC design tools (e.g. dc_shell, VCS) is a plus
- Attention to detail, innovative, enthusiastic and the ability to be a creative team player while working independently.
- Excellent spoken and written English

Responsibilities:

Interns will be working on developing our next generation Video ICs. Main duties include RTL design, verification and FPGA emulation.

Application method

Interested candidates please email resume, cover letter and transcripts to eleung@vixs.com, with title
"Application: ASIC Design Engineer - Internship"